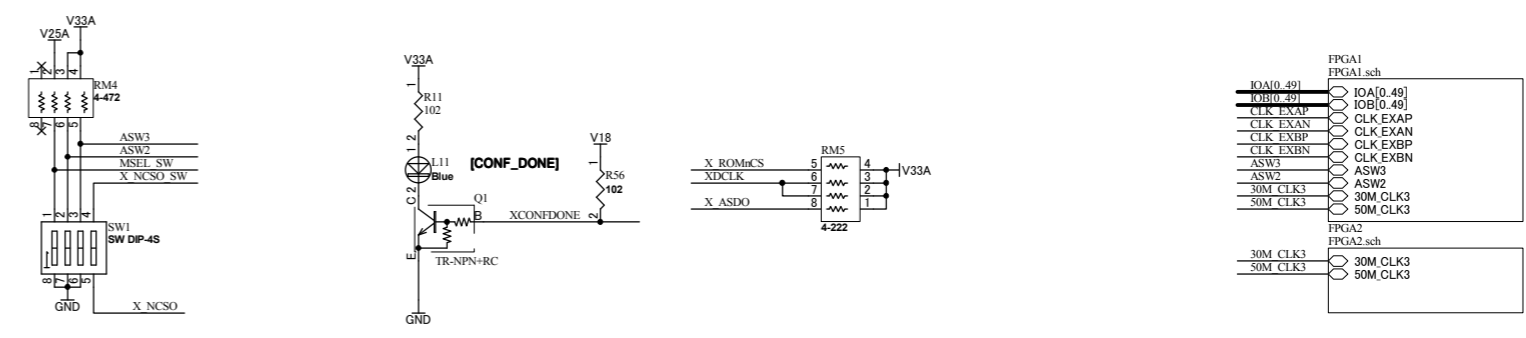
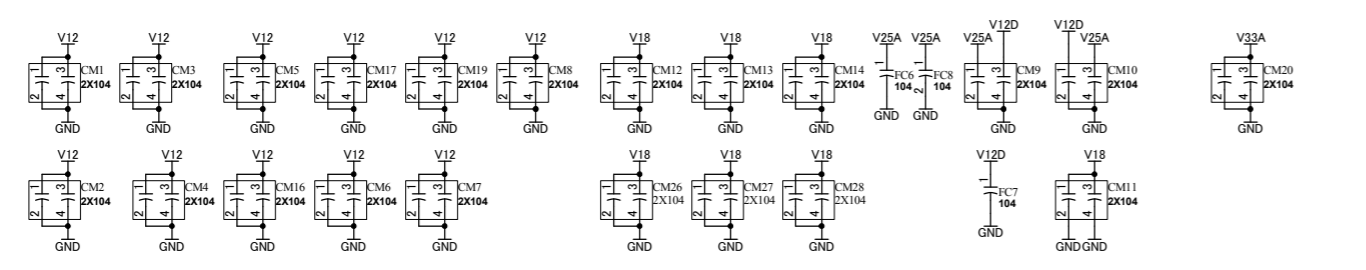
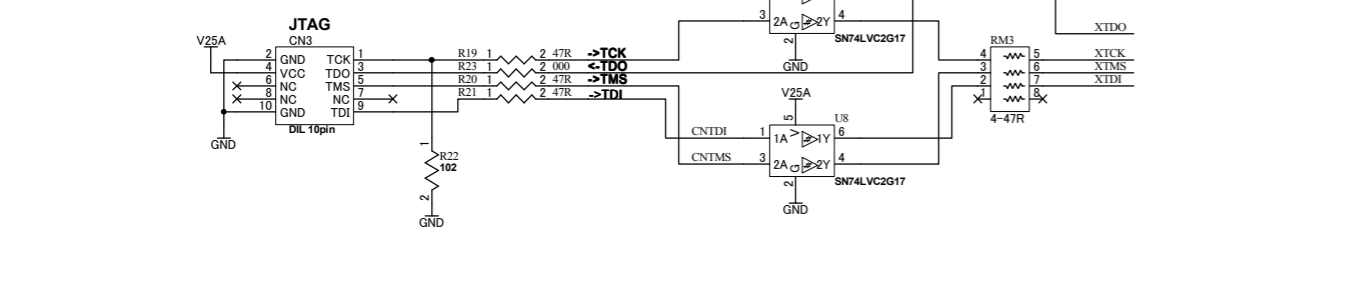
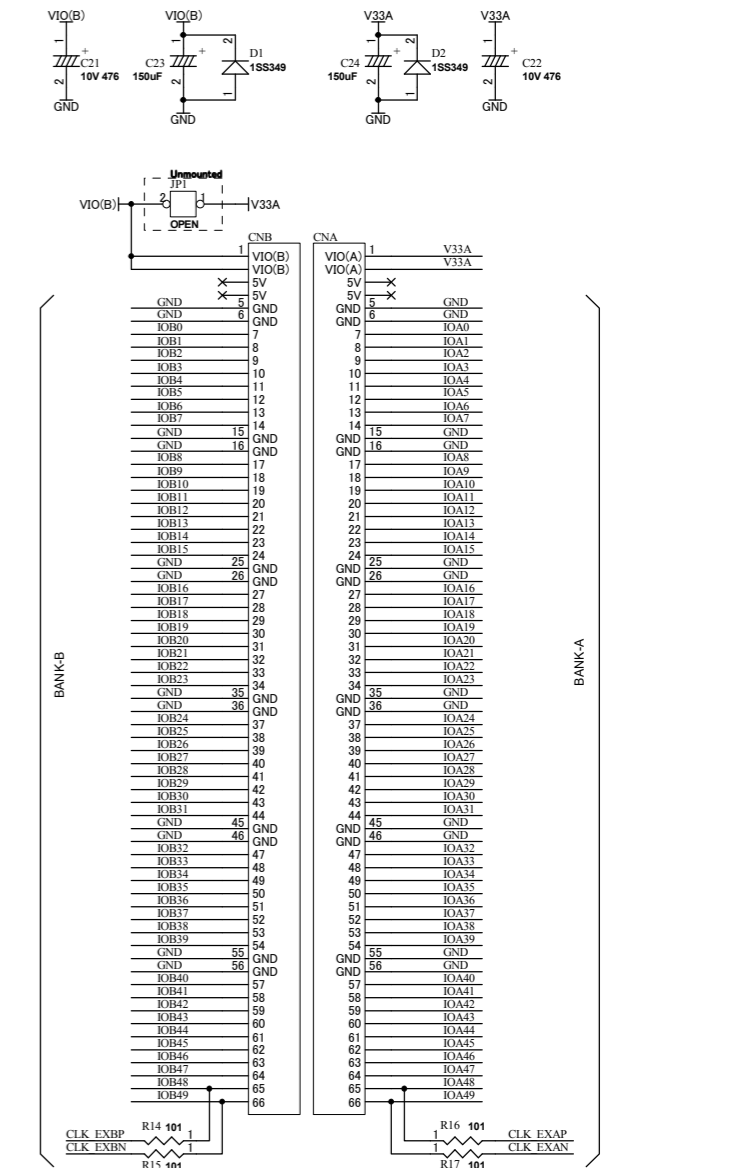
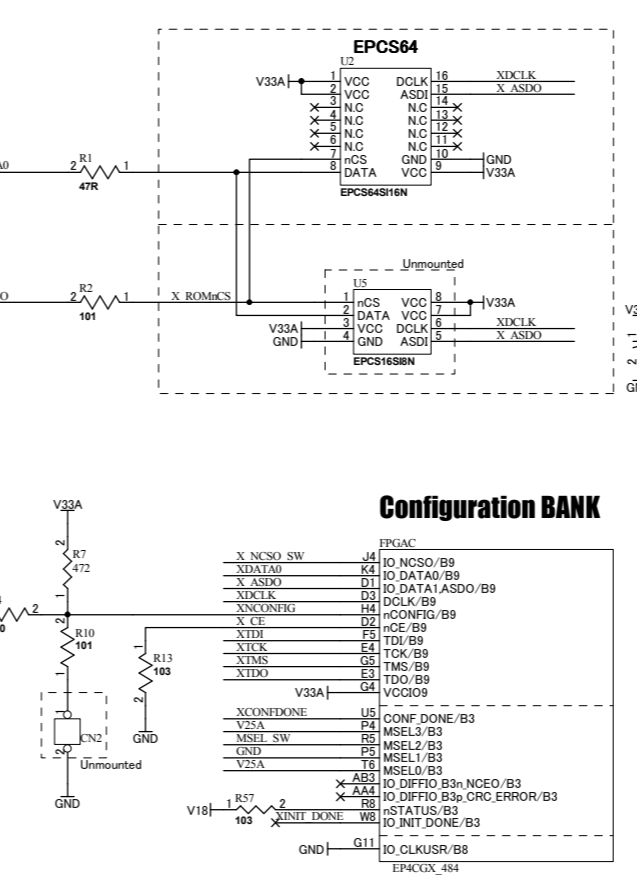
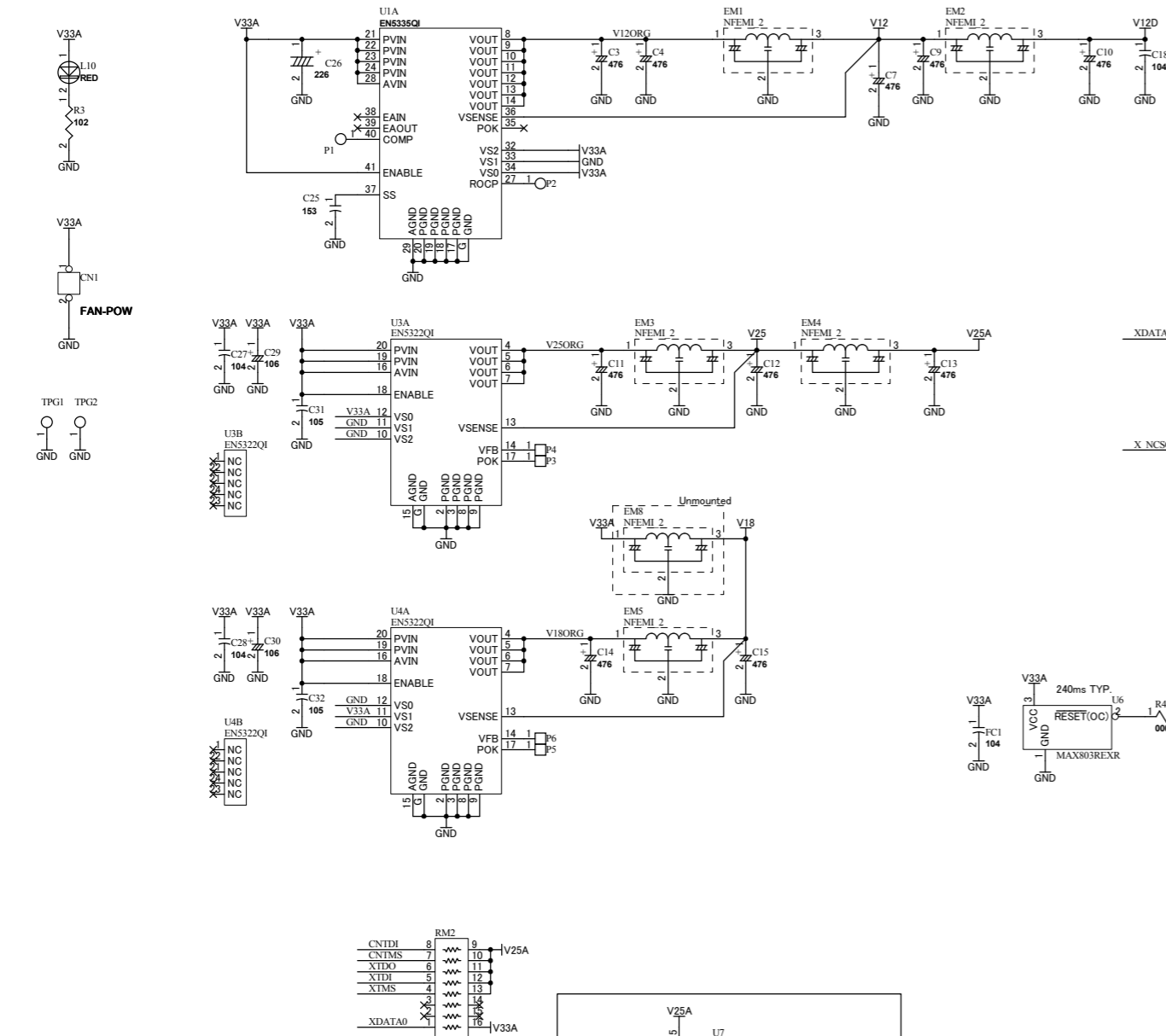
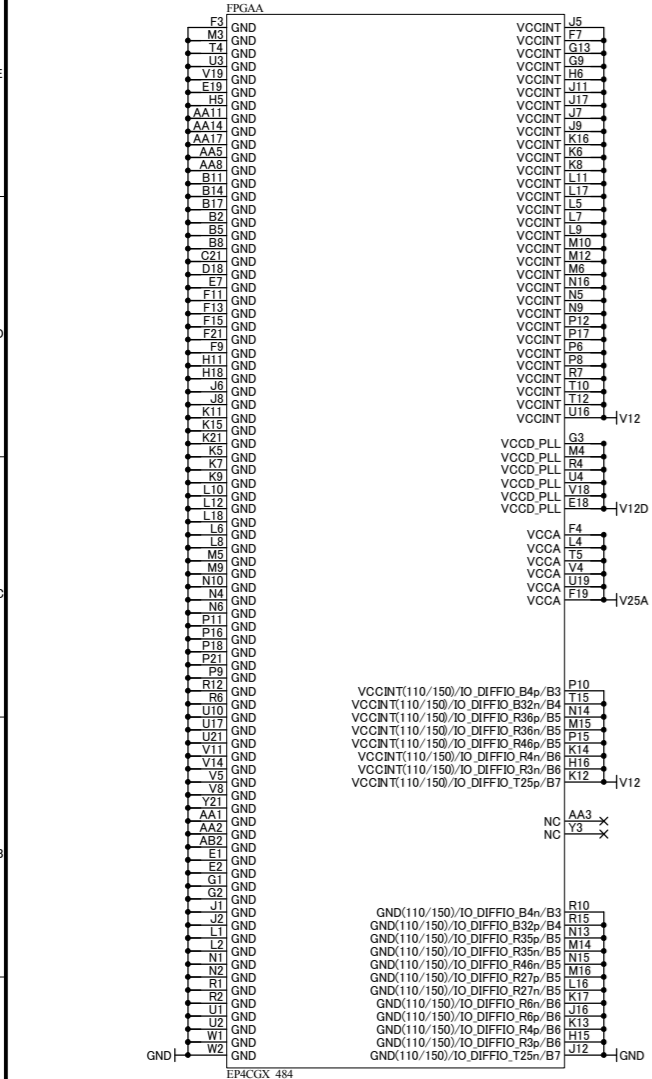
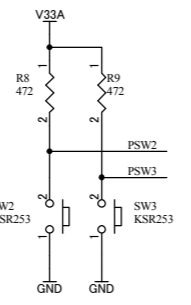
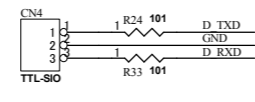
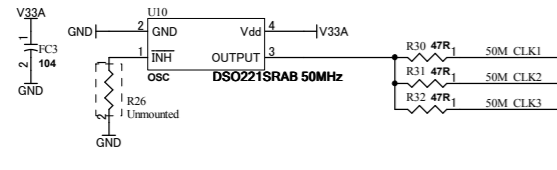
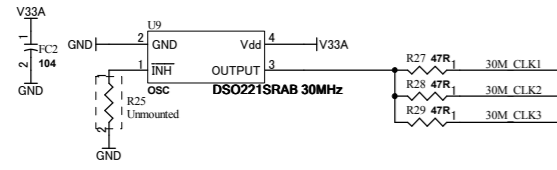
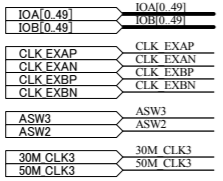
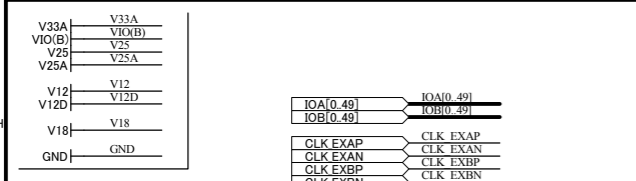


V33A	V33A
VIO(B)	VIO(B)
V25	V25
V25A	V25A
V12	V12
V12D	V12D
V18	V18
GND	GND

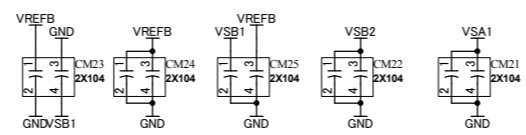


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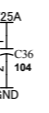


These pins are connected to VCCINT. You need to set them as INPUT.

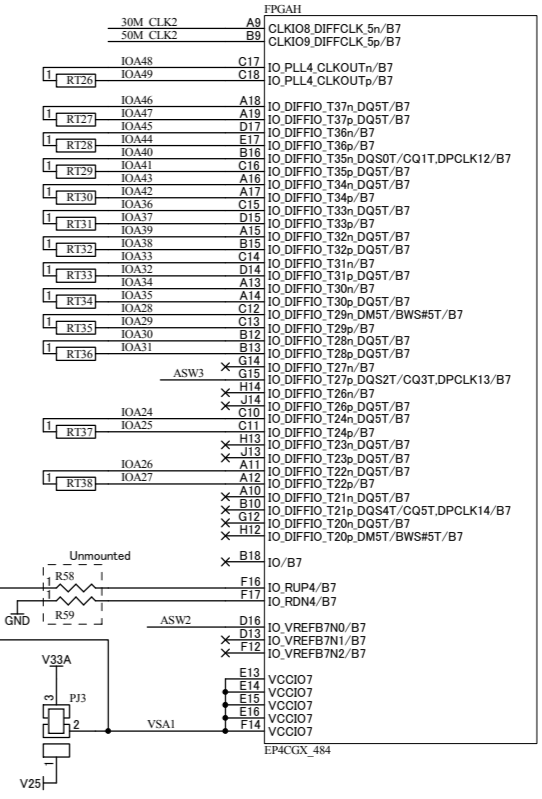
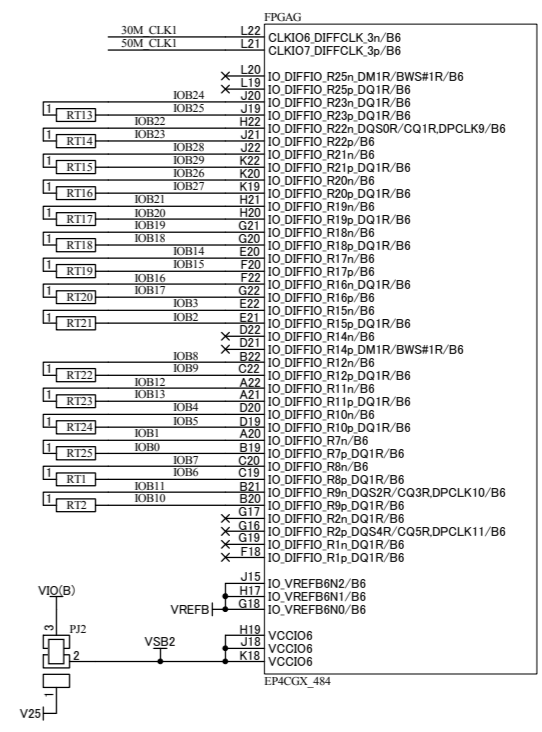
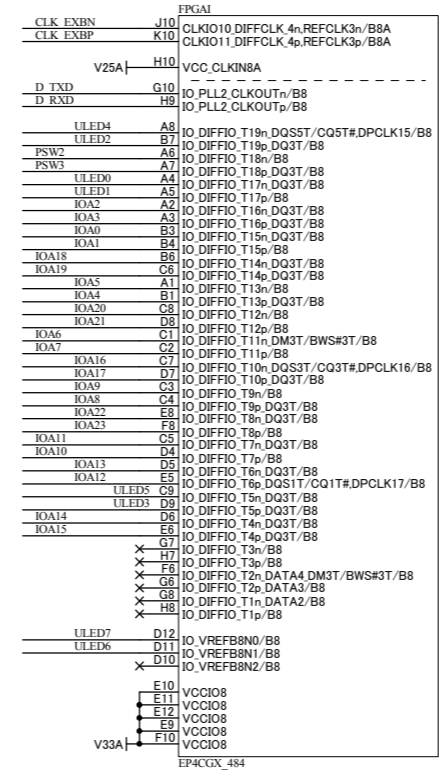
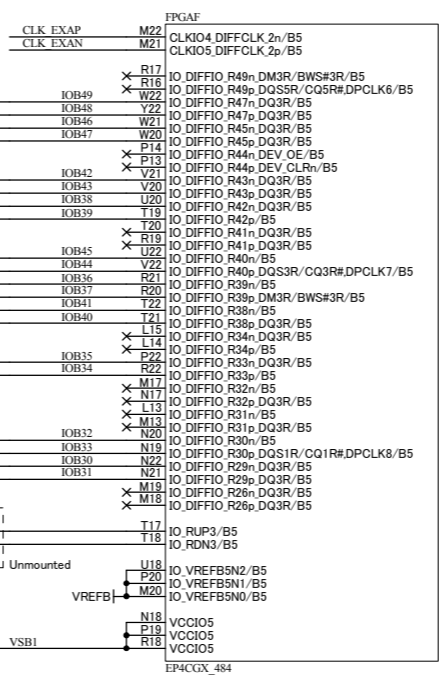
These pins are connected to GND. You need to set them as INPUT.



RIGHT EDGE IBANK 5/6I for CNB

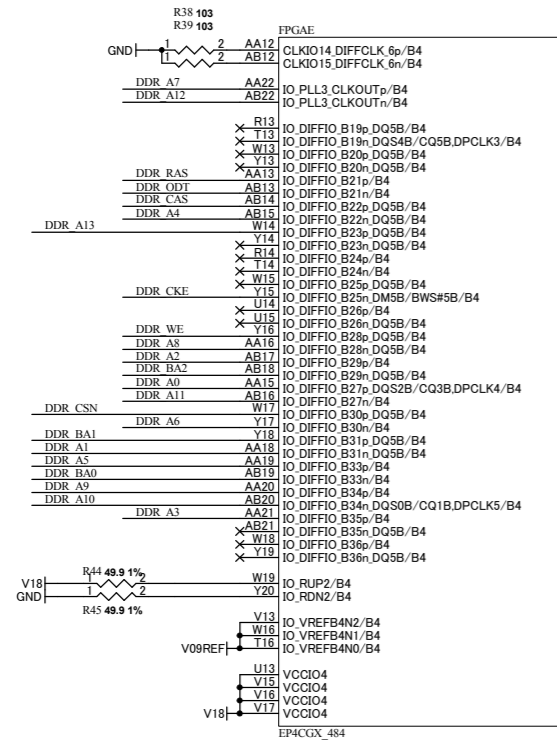


TOP EDGE IBANK 7/8I for CNA

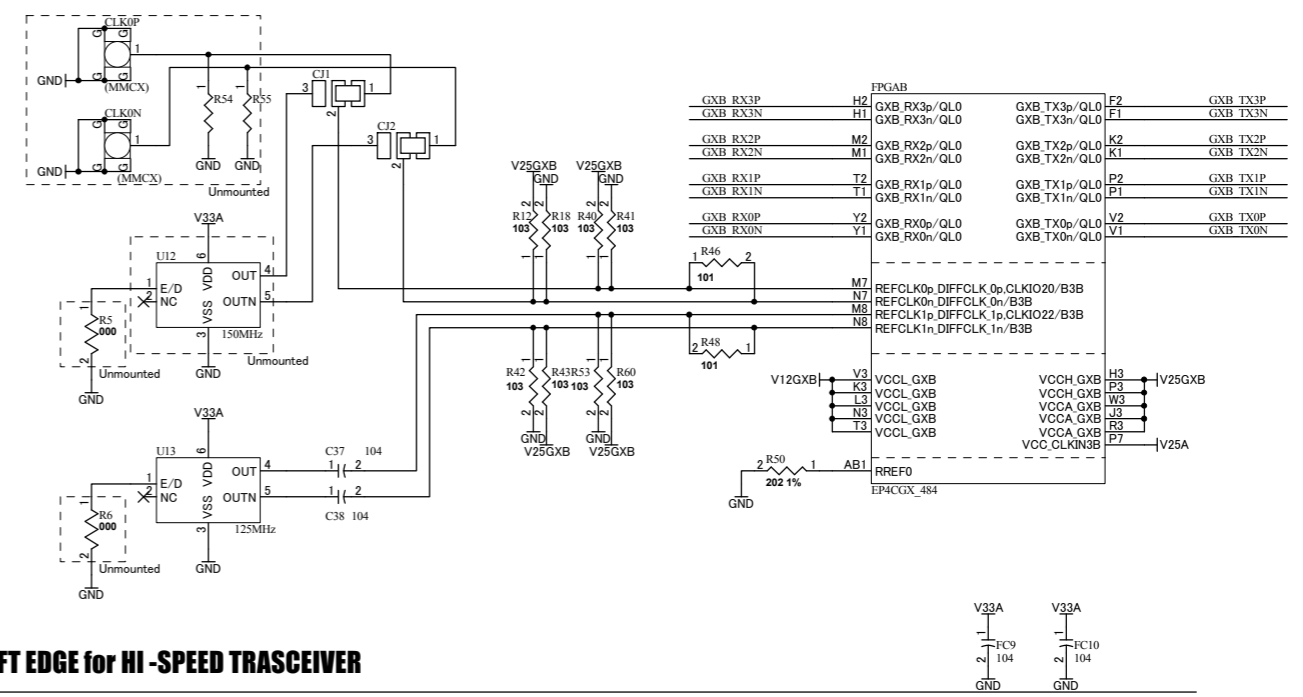
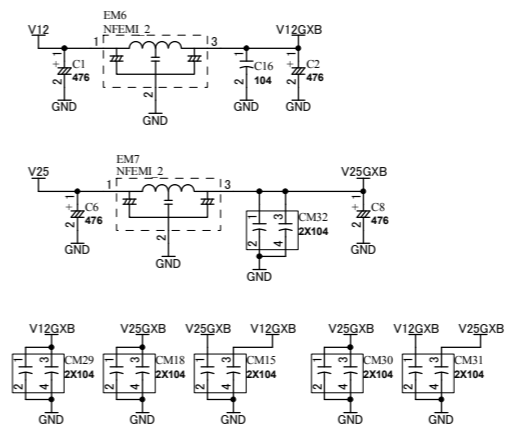
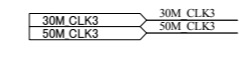
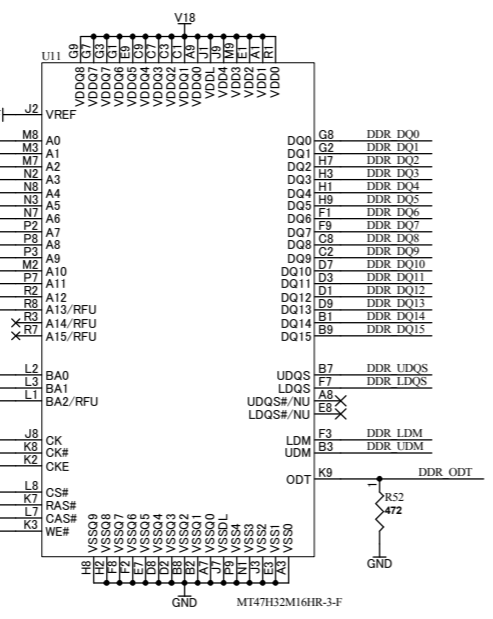
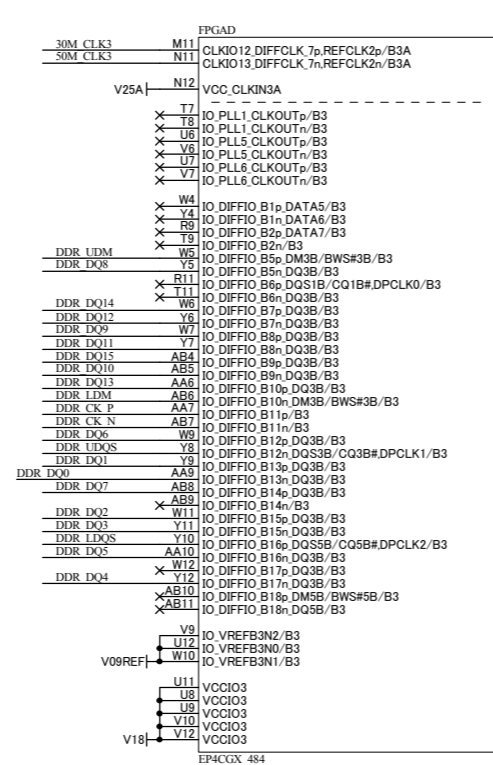


HUMAN DATA		ALTERA Cyclone IV GX F484 FPGA board	
HuMANDATA LTD. OSAKA JAPAN www.hdl.co.jp/en/(Global) www.hdl.co.jp/(Japan)		DOC. No. ACM-024	C1
Date: 20-Jun-2011 14:46:42	File: FPGA1.sch	Sheet 2	of 3

V33A	V33A
V10(B)	V10(B)
V25	V25
V25A	V25A
V12	V12
V12D	V12D
V18	V18
GND	GND

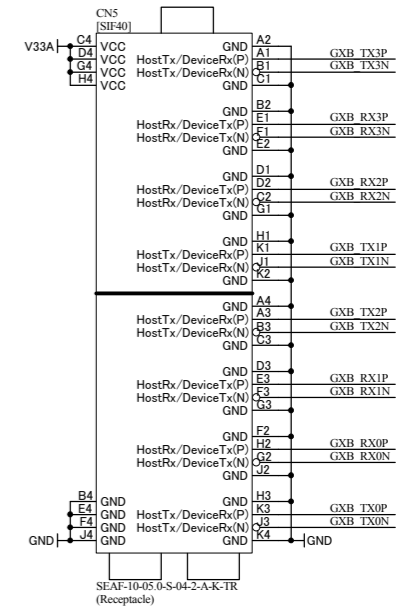


BOTTOM EDGE IBANK 3/4 for DDR2 SDRAM



LEFT EDGE for HI-SPEED TRASCEIVER

SIF40 Connector



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		ALTERA Cyclone IV GX F484 FPGA board	
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