

A

A

B

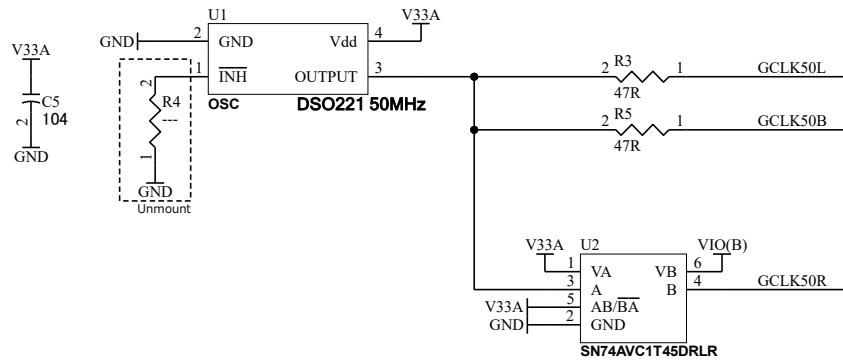
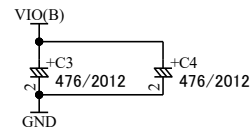
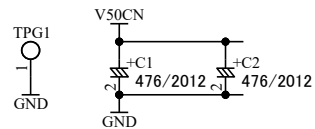
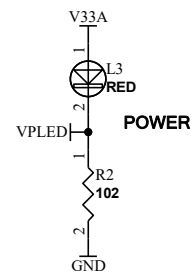
B

C

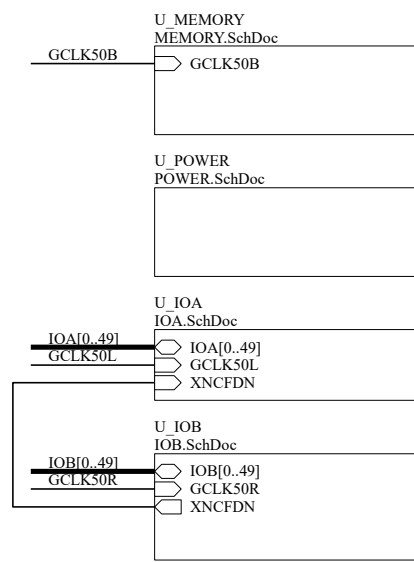
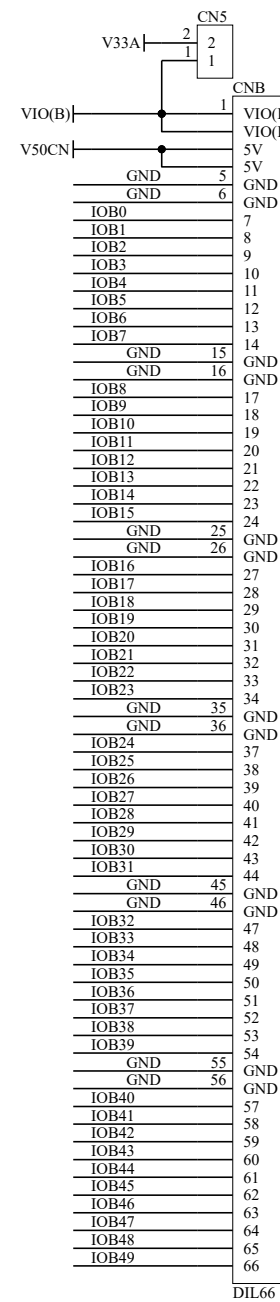
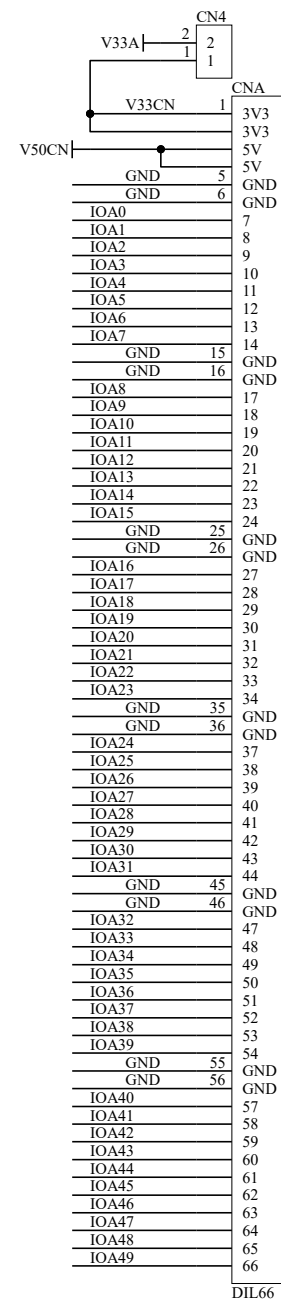
C

D

D



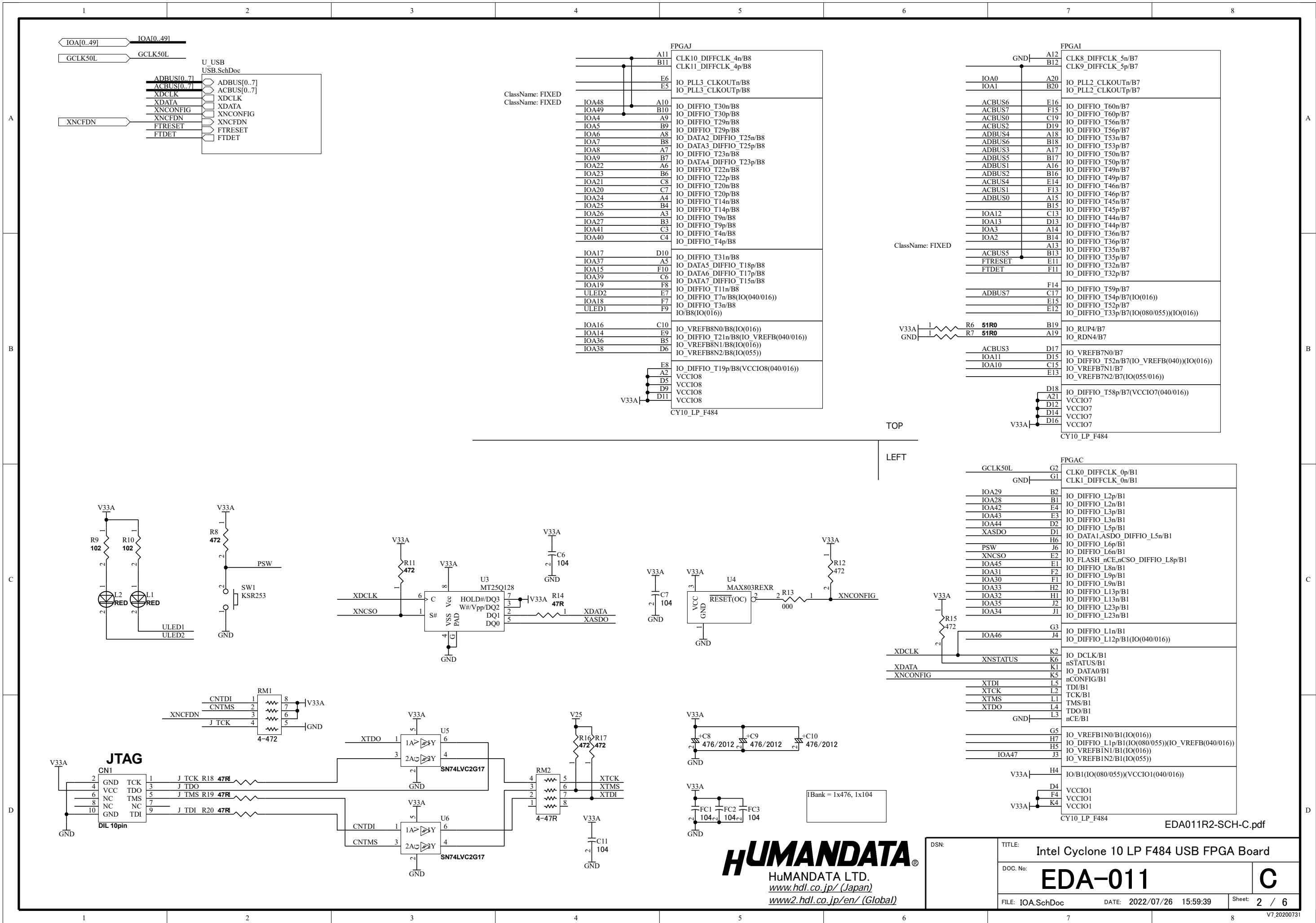
FPGAB		P14	
H3	IO_DIFFIO_L7n/B1(GND(040/016))	VCCINT(IO(016))	P14
J5	GND(IO(080/055/040))(GND(016))	VCCINT(IO(016))	N14
R3	IO_DIFFIO_L37n/B2(GND(040/016))	VCCINT(IO(016))	J16
AB6	IO_DIFFIO_B8p/B3(GND(040/016))	VCCINT(IO(016))	K15
Y15	IO_DIFFIO_B39n/B4(GND(040/016))	VCCINT(IO(016))	L16
T20	IO_DIFFIO_R45n/B5(GND(040/016))	VCCINT(IO(016))	M15
C18	IO_DIFFIO_T58n/B7(GND(040/016))	VCCINT(IO(016))	R12
D8	IO_DIFFIO_T19n/B8(GND(040/016))	VCCINT(IO(016))	R10
D7	IO_DIFFIO_T15p/B8(GND(016))	VCCINT(IO(016))	R8
Y21	GND(IO(080/055/040/016))	VCCINT(IO(016))	H9
U19	GND(IO(080/055/040/016))	VCCINT(IO(016))	G12
R18	GND(IO(080/055/040/016))	VCCINT(IO(016))	J8
J19	GND(IO(080/055/040/016))	VCCINT(IO(040))	M8
G7	GND(IO(080/055/040/016))	VCCINT(IO(040/016))	T7
		VCCINT(IO(040/016))	T9
F12	GND(IO(016))	VCCINT(IO(040/016))	T13
H12	GND(IO(016))	VCCINT(IO(040/016))	P15
H13	GND(IO(016))	VCCINT(IO(040/016))	H15
J15	GND(IO(016))	VCCINT(IO(040/016))	H11
K16	GND(IO(016))	VCCINT(IO(040/016))	K8
L15	GND(IO(016))	VCCINT(IO(055/040/016))	P17
N15	GND(IO(016))	VCCINT(IO(040/016))	L7
R13	GND(IO(016))	VCCINT(IO(055/040/016))	N16
R11	GND(IO(016))	VCCINT(IO(055/040/016))	K17
R9	GND(IO(016))	VCCINT(IO(055/040/016))	J17
P8	GND(IO(016))	VCCINT(IO(055/040/016))	G16
H14	GND(IO(040/016))	VCCINT(IO(055/040/016))	G14
H10	GND(IO(040/016))	VCCINT(IO(055/040/016))	G10
H8	GND(IO(040/016))	VCCINT(IO(055/040/016))	G8
N8	GND(IO(040))(GND(016))	VCCINT(IO(055/040/016))	J7
R7	GND(IO(040/016))	VCCINT(IO(055/040/016))	N7
T8	GND(IO(040/016))	VCCINT(IO(055/040/016))	P7
T12	GND(IO(040/016))	VCCINT(IO(055/040/016))	R6
P16	GND(IO(040/016))	VCCINT(IO(055/040/016))	U8
L8	GND(IO(040/016))	VCCINT(IO(055/040/016))	V7
G17	GND(IO(040/016))	VCCINT(IO(055/040/016))	T11
M7	GND(IO(055/040/016))	VCCINT(IO(055/040/016))	R15
F16	GND(IO(040/016))	VCCINT(IO(055/040/016))	G4
H16	GND(IO(055/040/016))	VCCINT(IO(080/055/040/016))	U15
G15	GND(IO(055/040/016))	VCCINT(IO(080/055/040/016))	U16
G13	GND(IO(055/040/016))	VCCINT(IO(080/055/040))	U17
G11	GND(IO(055/040/016))	VCCINT(IO(080/055/040))	R14
E10	GND(IO(055/040/016))	VCCINT(IO(080/055/040/016))	H17
G9	GND(IO(055/040/016))		
K7	GND(IO(055/040/016))		
P6	GND(IO(055/040/016))		
U7	GND(IO(055/040/016))		
V6	GND(IO(055/040/016))		
T10	GND(IO(055/040/016))		
U13	GND(IO(055/040/016))		
T14	GND(IO(055/040/016))		
N17	GND(IO(055/040/016))		
GND	CY10_LP_F484		



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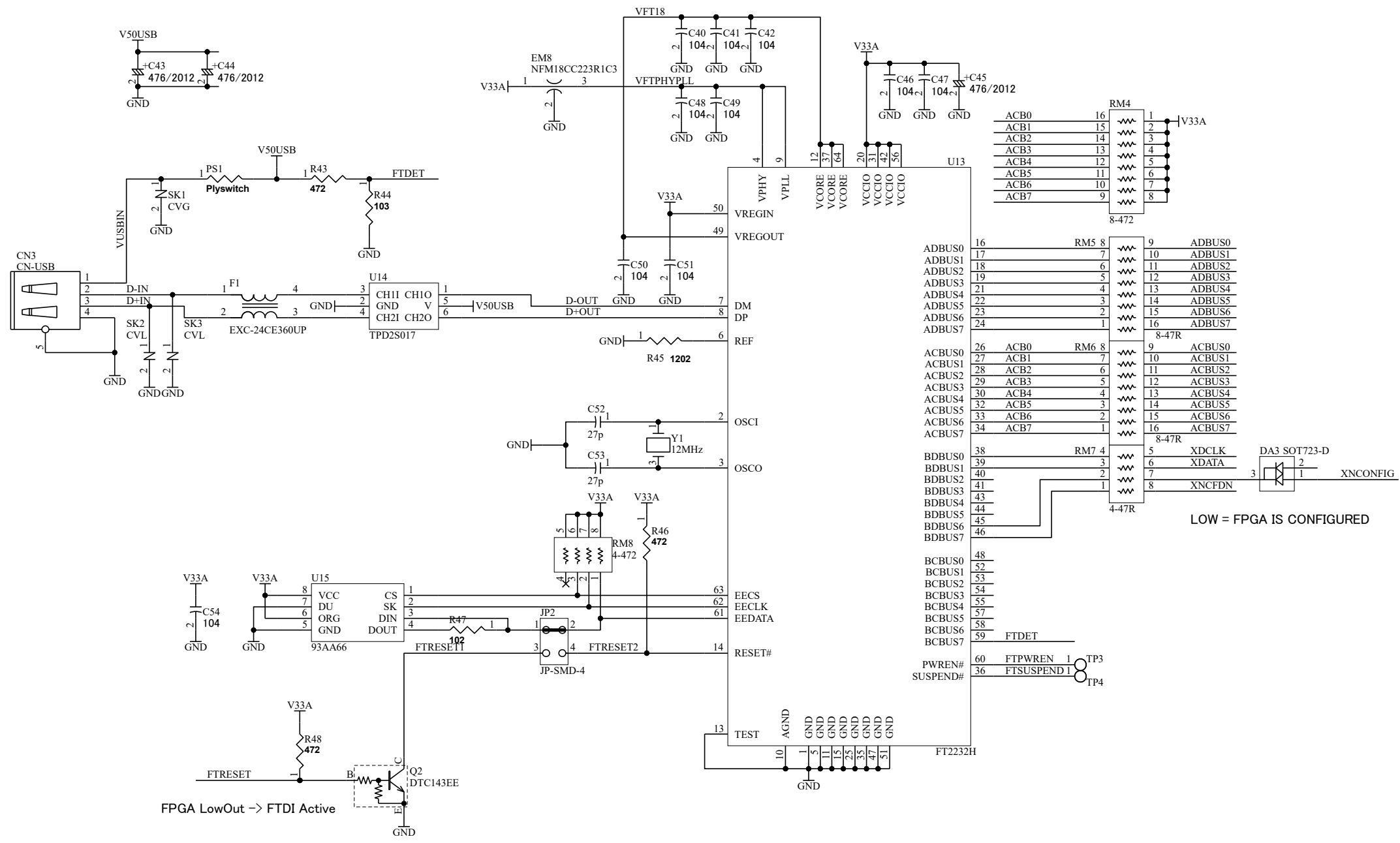
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DOC. No: <b>EDA-011</b>	<b>C</b>
FILE: EDA011C.SchDoc	DATE: 2022/07/26 15:59:39
Sheet: 1 / 6	



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DOC. No: <b>EDA-011</b>	<b>C</b>
FILE: IOA.SchDoc	DATE: 2022/07/26 15:59:39
Sheet: 2 / 6	V7.20200731

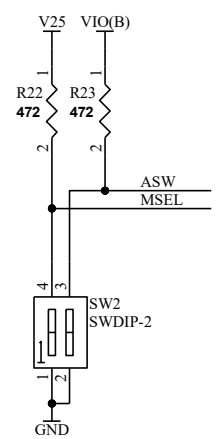
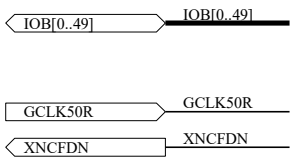
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ACBUS[0..7]	ACBUS[0..7]
XDCLK	XDCLK
XDATA	XDATA
XNCONFIG	XNCONFIG
XNCFDN	XNCFDN
FTDET	FTDET
FTRESET	FTRESET



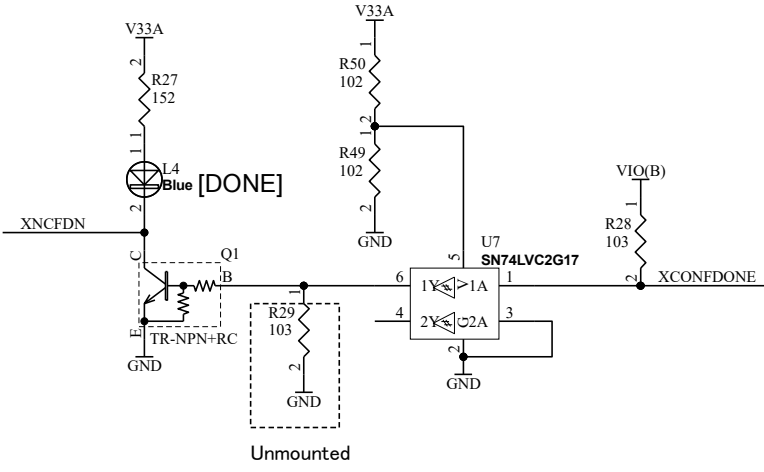
LOW = FPGA IS CONFIGURED



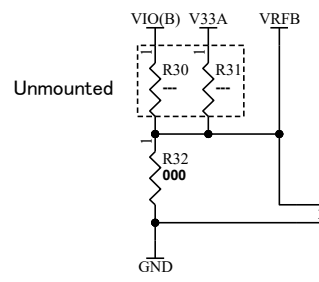
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FILE: USB.SchDoc	DATE: 2022/07/26 15:59:39
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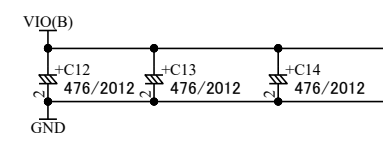
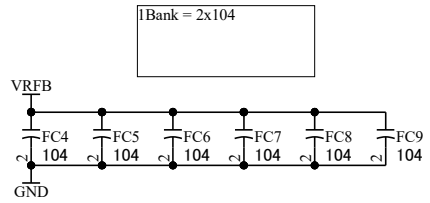
OFF = HIGH:AS  
ON = LOW:PS(JTAG)



Unmounted



Unmounted



IBank = 1x476, 1x104

FPGAD

T2	CLK2_DIFFCLK_1p/B2
T1	CLK3_DIFFCLK_1n/B2
L6	IO_DIFFIO_L25p/B2
M6	IO_DIFFIO_L25n/B2
M2	IO_DIFFIO_L27p/B2
M1	IO_DIFFIO_L27n/B2
M4	IO_DIFFIO_L28p/B2
M3	IO_DIFFIO_L28n/B2
N2	IO_DIFFIO_L29p/B2
N1	IO_DIFFIO_L29n/B2
P2	IO_DIFFIO_L30p/B2
P1	IO_DIFFIO_L30n/B2
R2	IO_DIFFIO_L31p/B2
R1	IO_DIFFIO_L31n/B2
P4	IO_DIFFIO_L33p/B2
P3	IO_DIFFIO_L33n/B2
U2	IO_DIFFIO_L34p/B2
U1	IO_DIFFIO_L34n/B2
V2	IO_DIFFIO_L35p/B2
V1	IO_DIFFIO_L35n/B2
W2	IO_DIFFIO_L38p/B2
W1	IO_DIFFIO_L38n/B2
Y2	IO_DIFFIO_L39p/B2
Y1	IO_DIFFIO_L39n/B2
T4	IO_DIFFIO_L48p/B2(IO(055/040/016))
T5	IO_DIFFIO_L48n/B2(IO(040))
N5	IO_DIFFIO_L32n/B2(IO(040/016))
N6	IO_DIFFIO_L36n/B2
V4	IO_RUP1/B2
V3	IO_RDN1/B2
T3	IO_VREFB2N1/B2
R5	IO_VREFB2N2/B2(IO(055/016))
P5	IO_DIFFIO_L36p/B2(IO_VREFB(040))(IO(016))
M5	IO_VREFB2N0/B2
R4	IO_DIFFIO_L37p/B2(VCCIO2(040/016))
N4	VCCIO2
U4	VCCIO2
W4	VCCIO2

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FPGAG

T22	CLK7_DIFFCLK_3n/B5
T21	CLK6_DIFFCLK_3p/B5
AA22	IO_DIFFIO_R51n/B5
AA21	IO_DIFFIO_R51p/B5
W22	IO_DIFFIO_R46n/B5
W21	IO_DIFFIO_R46p/B5
V22	IO_DIFFIO_R43n/B5
V21	IO_DIFFIO_R43p/B5
U22	IO_DIFFIO_R41n/B5
U21	IO_DIFFIO_R41p/B5
R22	IO_DIFFIO_R38n/B5
R21	IO_DIFFIO_R38p/B5
P22	IO_DIFFIO_R36n/B5
P21	IO_DIFFIO_R36p/B5
N22	IO_DEV_OE_DIFFIO_R29n/B5
N21	IO_DEV_CLRN_DIFFIO_R29p/B5
M22	IO_DIFFIO_R28n/B5
M21	IO_DIFFIO_R28p/B5
M20	IO_DIFFIO_R27n/B5
M19	IO_DIFFIO_R27p/B5
R20	IO_DIFFIO_R42n/B5(IO(016))
R19	IO_DIFFIO_R40p/B5
N20	IO_DIFFIO_R33n/B5
N18	IO_DIFFIO_R30p/B5
W20	IO_DIFFIO_R50n/B5(IO(080/055/040))
Y22	IO_DIFFIO_R49n/B5
U20	IO_DIFFIO_R48n/B5
T17	IO_RUP3/B5
T18	IO_RDN3/B5
W19	IO_VREFB5N2/B5(IO(016))
R17	IO_DIFFIO_R49p/B5(IO_VREFB(040/016))
P20	IO_VREFB5N1/B5
N19	IO_VREFB5N0/B5(IO(055/040/016))
M16	IO_DIFFIO_R48p/B5(IO(080/055/016))(IO_VREFB(040))
T19	IO_DIFFIO_R45p/B5(VCCIO5(040/016))
P18	VCCIO5
V19	VCCIO5
Y19	VCCIO5

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FPGAH

G22	CLK5_DIFFCLK_2n/B6
G21	CLK4_DIFFCLK_2p/B6
K22	IO_nCEO_DIFFIO_R23n/B6
K21	IO_CLKUSR_DIFFIO_R23p/B6
J22	IO_DIFFIO_R22n/B6
J21	IO_DIFFIO_R22p/B6
H22	IO_DIFFIO_R21n/B6
H21	IO_DIFFIO_R21p/B6
F22	IO_DIFFIO_R18n/B6
F21	IO_DIFFIO_R18p/B6
H20	IO_DIFFIO_R16n/B6
H19	IO_DIFFIO_R16p/B6
E22	IO_DIFFIO_R15n/B6
E21	IO_DIFFIO_R15p/B6
D22	IO_DIFFIO_R14n/B6
D21	IO_DIFFIO_R14p/B6
F20	IO_DIFFIO_R13n/B6
F19	IO_DIFFIO_R13p/B6
C22	IO_DIFFIO_R10n/B6
C21	IO_DIFFIO_R10p/B6
B22	IO_DIFFIO_R9n/B6
B21	IO_DIFFIO_R9p/B6
L22	IO_INIT_DONE_DIFFIO_R24n/B6
L21	IO_CRC_ERROR_DIFFIO_R24p/B6
M18	CONF_DONE/B6
M17	MSEL0/B6
L18	MSEL1/B6
L17	MSEL2/B6
K20	MSEL3/B6
K18	IO_DIFFIO_R20n/B6
G18	IO_DIFFIO_R12n/B6
C20	IO_DIFFIO_R8n/B6
F17	IO_DIFFIO_R2n/B6
J18	IO_DIFFIO_R20p/B6(IO_VREFB(040))(IO(016))
K19	IO_VREFB6N2/B6
H18	IO_VREFB6N1/B6
D20	IO_VREFB6N0/B6(IO(055/016))
J20	IO_DIFFIO_R17n/B6(VCCIO6(040/016))
E19	VCCIO6
G19	VCCIO6
L19	VCCIO6

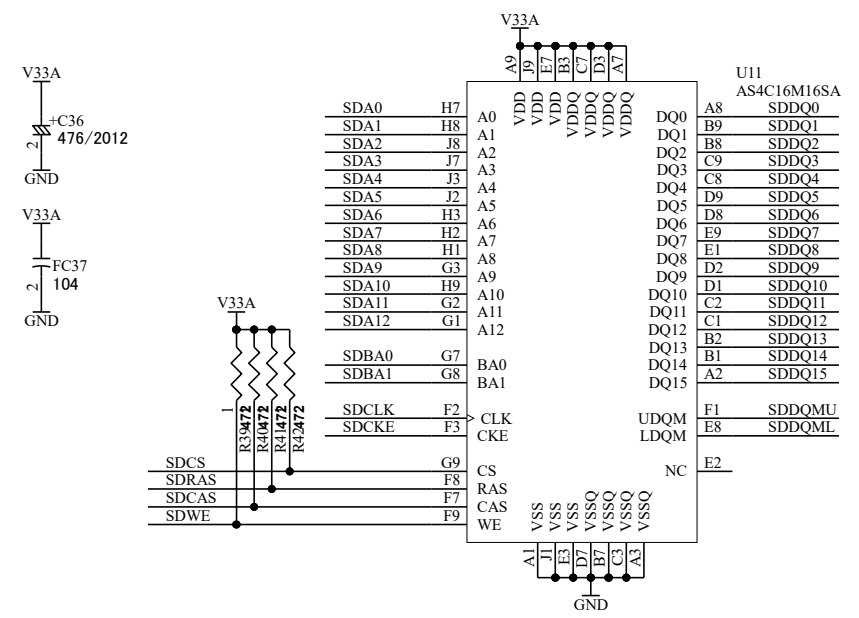
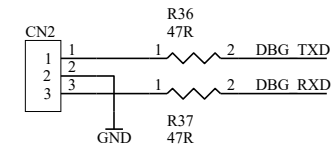
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GCLK50B GCLK50B



FPGA E	
GCLK50B	AA11
GND	AB11
DBG RXD	AA3
DBG TXD	AB3
SDA5	W7
SDDQ8	Y7
SDDQ10	AA7
SDDQ9	AB7
SDDQ12	AA8
SDDQ11	AB8
SDDQ15	AA9
SDDQ14	AB9
W10	
SDA9	Y10
S D1	V8
SDA4	W8
SDA6	V10
S D0	U10
SDDQ0	AA10
SDDQ13	AB10
SDA8	Y3
SDA7	W6
SDA11	AA5
SDDQMU	AB5
S CLK	V5
S CS	Y6
SDA12	AA4
S D3	U9
S D2	Y8
SDCKE	V11
	V9
	U11
	Y4
	AB4
	AA6
	AB2
	W5
	W9
	W11

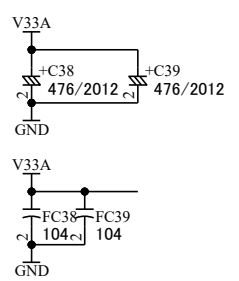
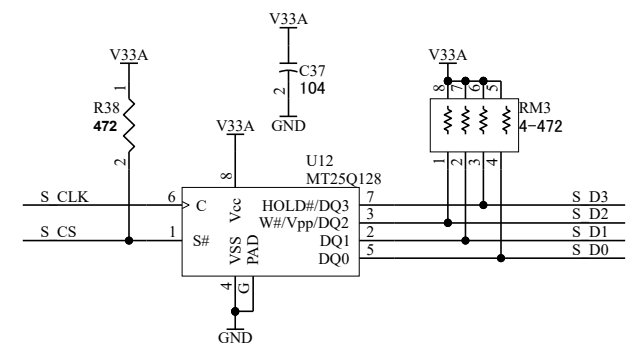
FPGA E

CLK15_DIFFCLK_6p/B3	AA12
CLK14_DIFFCLK_6n/B3	AB12
IO_PLL1_CLKOUTp/B3	T16
IO_PLL1_CLKOUTn/B3	R16
IO_DIFFIO_B9p/B3	AA13
IO_DIFFIO_B9n/B3	AB13
IO_DIFFIO_B14p/B3	AA14
IO_DIFFIO_B14n/B3	AB14
IO_DIFFIO_B17p/B3	W13
IO_DIFFIO_B17n/B3	Y13
IO_DIFFIO_B18p/B3	AA15
IO_DIFFIO_B18n/B3	AB15
IO_DIFFIO_B23p/B3	AA16
IO_DIFFIO_B23n/B3	AB16
IO_DIFFIO_B13p/B3	V8
IO_DIFFIO_B13n/B3(IO(080/055/040/016))	W8
IO_DIFFIO_B15p/B3(IO(016))	V10
IO_DIFFIO_B15n/B3	U10
IO_DIFFIO_B24p/B3	AA10
IO_DIFFIO_B24n/B3(IO(016))	AB10
IO_DIFFIO_B3n/B3	Y3
IO_DIFFIO_B4p/B3	W6
IO_DIFFIO_B5p/B3	AA5
IO_DIFFIO_B8n/B3	AB5
IO_DIFFIO_B1n/B3	V5
IO/B3(IO(040/016))	Y6
IO/B3(IO(016))	AA4
IO_DIFFIO_B12n/B3	U9
IO/B3(IO(080/055/040/016))	Y8
IO/B3(IO(055/040/016))	V11
IO_VREFB3N1/B3	V9
IO_VREFB3N0/B3(IO(055/016))	U11
IO_VREFB3p/B3(IO_VREFB(040/016))	Y4
IO_VREFB3N2/B3(IO(016))	AB4
IO_DIFFIO_B7n/B3(VCCIO3(040/016))	AA6
VCCIO3	AB2
VCCIO3	W5
VCCIO3	W9
VCCIO3	W11

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FPGA F	
CLK13_DIFFCLK_7p/B4	AA12
CLK12_DIFFCLK_7n/B4	AB12
IO_PLL4_CLKOUTp/B4	T16
IO_PLL4_CLKOUTn/B4	R16
IO_DIFFIO_B32p/B4	AA13
IO_DIFFIO_B32n/B4	AB13
IO_DIFFIO_B35p/B4	AA14
IO_DIFFIO_B35n/B4	AB14
IO_DIFFIO_B36p/B4	W13
IO_DIFFIO_B36n/B4	Y13
IO_DIFFIO_B37p/B4	AA15
IO_DIFFIO_B37n/B4	AB15
IO_DIFFIO_B40p/B4	AA16
IO_DIFFIO_B40n/B4	AB16
IO_DIFFIO_B44p/B4	U14
IO_DIFFIO_B44n/B4	V15
IO_DIFFIO_B48p/B4	W17
IO_DIFFIO_B48n/B4	Y17
IO_DIFFIO_B49p/B4	AA20
IO_DIFFIO_B49n/B4	AB20
IO_DIFFIO_B41p/B4(IO(040/016))	V13
IO_DIFFIO_B43p/B4	V14
IO_DIFFIO_B45p/B4	W15
IO_DIFFIO_B46n/B4	T15
IO_DIFFIO_B38p/B4	AB18
IO_RUP2/B4	U12
IO_RDN2/B4	AB19
IO_VREFB4N2/B4(IO(016))	V12
IO_DIFFIO_B41n/B4(IO_VREFB(040/016))	W14
IO_VREFB4N1/B4(IO(016))	AA18
IO_VREFB4N0/B4(IO(055))	V16
IO_DIFFIO_B39p/B4(VCCIO4(040/016))	Y14
VCCIO4	AB21
VCCIO4	W12
VCCIO4	W16
VCCIO4	W18

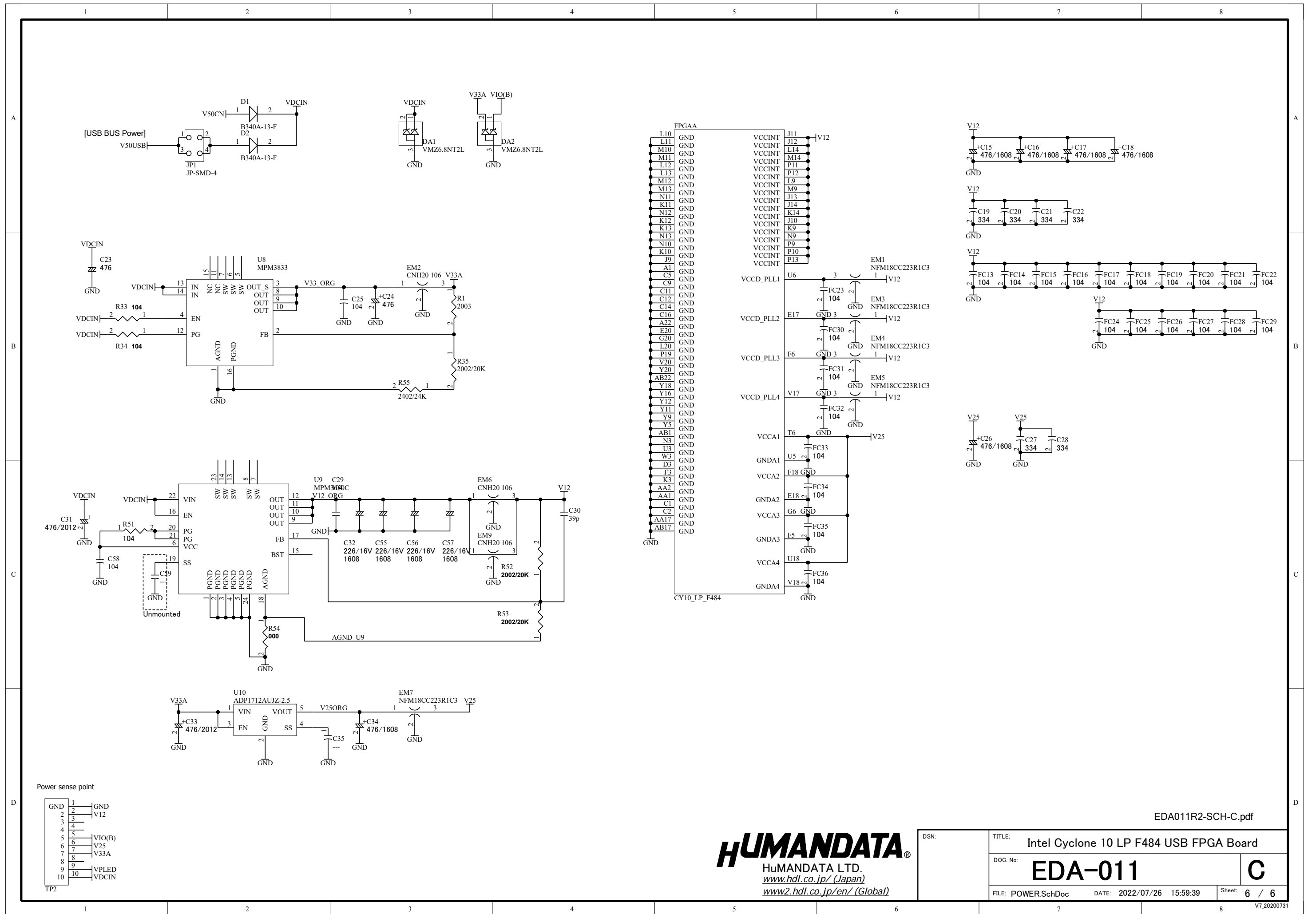
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DSN:	TITLE: Intel Cyclone 10 LP F484 USB FPGA Board
DOC. No:	<b>EDA-011</b>
FILE: MEMORY.SchDoc	DATE: 2022/07/26 15:59:39
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DOC. No:	<b>EDA-011</b>
FILE: POWER.SchDoc	DATE: 2022/07/26 15:59:39
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